Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method for providing an external clock signal to an internal memory block of a self-timed memory, the method comprising:

receiving an internal clock signal from a clock monitor of the self-timed memory;

receiving an external clock signal, wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal;

receiving a control signal; ~~and,~~ and

providing, in dependence upon the control ~~signal~~ signal, the internal clock signal to the internal memory block during a normal mode of operation of the self-timed memory, and the external clock signal to the internal memory block during a test mode of the self-timed memory.

2. (currently amended) A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 1 ~~wherein~~ further comprising switching provision of the external clock signal received during test mode ~~is generated~~ to different internal memory blocks according to a predetermined test pattern.

3. (currently amended) A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 2 wherein the duty cycle of the external clock signal received during test mode comprises a duty cycle lower than a 50% duty cycle of the internal memory block.

4. (currently amended) A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 2 wherein the duty cycle of the external clock signal received during test mode comprises a duty cycle higher than a 50% duty cycle of the internal memory block.

5. (currently amended) A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 1 ~~wherein~~ further comprising providing the internal clock signal ~~is provided~~ to the internal memory block in ~~absence of a~~ an absence of the control signal.

6. (currently amended) A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 1 wherein receiving the control signal further comprises receiving a control signal indicating initiation of the test mode ~~is provided~~.

7. (currently amended) A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 6 wherein receiving the control signal further comprises receiving a control signal indicating termination of the test mode ~~is provided~~.

8. (currently amended) A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 7 wherein receiving the control signal further comprises receiving the ~~at least a~~ control signal ~~is provided~~ during the test mode.

9. (currently amended) A self-timed memory comprising:

an internal memory ~~block~~ block;

a clock monitor for receiving an external clock signal and for providing ~~an internal clock signal in dependence thereupon~~ a clock signal to the internal memory block;

a test system interposed between the clock monitor and the internal memory block, the test system comprising:

an internal clock signal input port in signal communication with the clock monitor for receiving ~~the~~ an internal clock signal;

an external clock signal input port for receiving the external clock signal, wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal;

a control signal input port for receiving a control signal;

an output port in signal communication with the internal memory block; ~~and,~~ and

a multiplexer in signal communication with the internal clock signal input port, the external clock signal input ~~port~~ port, the control signal input ~~port~~ port, and the output port, ~~the control circuitry for receiving~~ wherein the multiplexer is configured to receive the internal clock signal, the external clock signal, and the control ~~signal, and~~ signal;

~~for providing,~~ wherein the multiplexer is further configured to provide, in dependence upon the control signal, the internal clock signal via the output port to the internal memory block during a normal mode of operation of the self-timed memory, and ~~for providing~~ the external clock signal to the internal memory block during a test mode of the self-timed memory.

10. (original) A self-timed memory as defined in claim 9 wherein the clock monitor comprises an input port for receiving the external clock signal and wherein the input port is connected to the external clock signal input port of the test system.

11. (currently amended) A self-timed memory as defined in claim 10 comprising test circuitry in signal communication with the test system, the test circuitry for providing ~~a control~~ the control signal to the test system and for providing the external clock signal to the test system during ~~test~~ the test mode.

12. (original) A self-timed memory as defined in claim 9 wherein the internal memory block comprises an address decoder.

13. (original) A self-timed memory as defined in claim 9 wherein the internal memory block comprises a sense amplifier.

14. (currently amended) A self-timed memory as defined in claim 9 wherein the internal memory block comprises a column and bank ~~decoder~~ decoder.

15. (original) A self-timed memory as defined in claim 9 wherein the internal memory block comprises a precharge and discharge circuitry.

16. (original) A self-timed memory as defined in claim 9 wherein the internal memory block comprises input/output latches.

17. (currently amended) A self-timed memory comprising:

~~at least~~ an internal memory block;

a clock monitor for receiving an external clock signal and for providing ~~at least an internal clock signal in dependence thereupon~~ a clock signal to the ~~at least an~~ internal memory block;

a test system interposed between the clock monitor and the ~~at least an~~ internal memory block, the test system comprising:

~~at least~~ an internal clock signal input port in signal communication with the clock monitor for receiving ~~at least~~ an internal clock signal;

an external clock signal input port for receiving the external clock signal, wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal;

a control signal input port for receiving a control signal;

~~at least~~ an output port in signal communication with the ~~at least an~~ internal memory block; ~~and,~~ and

control circuitry in signal communication with the ~~at least an~~ internal clock signal input port, the external clock signal input port, the control signal input port and the ~~at least an~~ output port, wherein the control circuitry ~~for receiving~~ is configured to receive the ~~at least an~~ internal clock signal, the external clock signal, and the control ~~signal, and~~ signal;

~~for providing,~~ wherein the control circuitry is further configured to provide, in dependence upon the control signal, the ~~at least an~~ internal clock signal via the ~~at least an~~ output port to the ~~at least an~~ internal memory block during a normal mode of operation of the self-timed memory, and ~~for providing~~ the external clock signal to ~~at least one of~~ the ~~at least an~~ internal memory block during a test mode of the self-timed memory.

18. (original) A self-timed memory as defined in claim 17 wherein the control circuitry comprises a multiplexer.

19. (currently amended) A self-timed memory as defined in claim 18 wherein the ~~at least an~~ internal memory block comprises an address decoder.

20. (currently amended) A self-timed memory as defined in claim 19 wherein the ~~at least an~~ internal memory block comprises a sense amplifier.

21. (currently amended) A self-timed memory as defined in claim 20 wherein the ~~at least an~~ internal memory block comprises a column and bank decoder.

22. (currently amended) A self-timed memory as defined in claim 21 wherein the ~~at least an~~ internal memory block comprises a precharge and discharge circuitry.

23. (currently amended) A self-timed memory as defined in claim 22 wherein the ~~at least an~~ internal memory block comprises input/output latches.

24. (currently amended) A self-timed memory as defined in claim 23 further comprising test circuitry in signal communication with the test system, the test circuitry for providing ~~a control~~ the control signal to the test system and for providing the external clock signal to the test system during ~~test~~ the test mode.